Xilinx Verilog < Design Suite Version: 14.1> Tutorial

Department of Electrical and Computer Engineering State University of New York – New Paltz

1. Start A New Project.

> ISE Project Navigator (P.15xf)						
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Start Image:						
Console	+□₽×					
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Click Next.

Make Sure the Device Properties are chosen as shown below.

New Project Wizard		
Project Settings		
pecify device and project properties.		
elect the device and design flow for the pr	roject	
Property Name	Value	
Evaluation Development Board	None Specified	
Product Category	All	•
Family	Spartan3E	1
Device	XC3S500E	
Package	FG320	•
Speed	-4	
Top-Level Source Type	HDL	
Synthesis Tool	XST (VHDL/Verilog)	•
Simulator	ISim (VHDL/Verilog)	•
Preferred Language	Verilog	
Property Specification in Project File		
Manual Compile Order		
VHDL Source Analysis Standard	VHDL-93	
Enable Message Filtering		_
ore Info	Next Can	IC

Click Next. Click finish.

2. Go to **Project** <- **New Source**

On the New Source Wizard, click on **Verilog module** and type a filename.

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<u>.</u>		and the second se				
		New Source Wizard				
		Select Source Type				
-		Select source type, file name and its location.				
		IP (CORE Generator & Architecture Wizard) Schematic				
		User Document				
		Verilog Module				
		Verilog Test Fixture	le name:			
		📘 🚺 VHDL Library				
\blacktriangleright	3	VHDL Test Bench	AdderVerilog			
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			Add to project			
	More Info Next Cancel					

Click "Next". Click "Finish".

3. In this exercise, you are designing a full adder with X, Y, and Z as inputs and S and C as outputs. Hence, set the ports accordingly.

G	New Source Wizard						x
Defin	ne Module						
	y ports for module. Name AdderVerilog						
	Port Name	Directio	n	Bus	MSB	LSB	-
х		input	-				
Y		input	-				
Z		input	-				
S		output	-				
С		output	-				Ξ
		input	-				
		input	-				
		input	-				
		input	-				
		input	-				_
		input	-				-
More In	ſſŎ			C	Next	Cancel	

Click "Next"

Click "Finish"

4. This will open the editor where you can input your VHDL code.

File Edit View Project Source Process Tools Windo	w Layou	t Help
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esign ↔□♂×		1 `timescale 1ns / 1ps
🍸 View: 💿 🄯 Implementation 🔘 🧱 Simulation	ÞE	2 /////////////////////////////////////
Hierarchy		3 // Company:
	=	4 // Engineer:
☐	2	5 //
AdderVerilog.v)	Ξ	6 // Create Date: 09:12:13 04/10/2013 7 // Design Name:
—		8 // Module Name: AdderVerilog
	2	9 // Project Name:
23	1	10 // Target Devices:
		11 // Tool versions:
		12 // Description:
	%	13 //
1	*	14 // Dependencies:
		15 //
		<pre>16 // Revision:</pre>
		17 // Revision 0.01 - File Created
		<pre>18 // Additional Comments:</pre>
		19 // 20 /////////////////////////////////
		20 ////////////////////////////////////
		22 input X,
No Processes Running		23 input Y,
		24 input Z,
T Processes: AdderVerilog		25 output S,
💥 📃 Design Summary/Reports		26 output C
— 😥 💥 🛛 Design Utilities		27);
		28
		29
i inperiencoesign		30 endmodule
Generate Programming File		31
Configure Target Device		
& Analyze Design Using ChipScope		

Note that

$$\begin{split} S &= X \oplus Y \oplus Z \\ C &= XY + YZ + XZ \end{split}$$

Hence, you may add appropriate equations to the module. Note the following operators

	and
~&	nand
	or
~	nor
٨	xor
^~ or ~^	xnor

 $S = X^{\Lambda}Y^{\Lambda}Z$

 $C=(X\&Y) \mid (Y\&Z) \mid (X\&Z)$

```
1 `timescale 1ns / 1ps
// Company:
3
4
  // Engineer:
  11
5
  // Create Date:
                09:12:13 04/10/2013
6
7 // Design Name:
8 // Module Name: AdderVerilog
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
  ______
20
21 module AdderVerilog(
22
     input X,
     input Y,
23
     input Z,
24
     output S,
25
      output C
26
27
      );
28 assign S = X^Y^Z;
29
  assign C= (X \& Y) | (Y \& Z) | (X \& Z);
30
31
32
   endmodule
33
```

5. Save the file.

The project can be simulated using ISIM simulator as described in its tutorial

When the design is completed, open the User Constraints Editor and assign the pins to the correct inputs and outputs. Follow the steps in the Download Tutorial to complete the process.